WHAT IS CLAIMED IS:

1. A thin film resistor device, comprising:

a resistive layer located on a first dielectric layer;

first and second contact pads located on the resistive layer; and

a second dielectric layer located over the resistive layer and the first and second contact pads.

2. The thin film resistor as recited in Claim 1 further including a first interconnect that contacts the first contact pad and a second interconnect that contacts the second contact pad.

3. The thin film resistor as recited in Claim 2 further including interconnect metallization structures wherein the first dielectric layer is located between the interconnect metallization structure and the resistive layer.

4. The thin film resistor as recited in Claim 3 wherein each of the first and second interconnects contact an interconnect metallization structure.

5. The thin film resistor as recited in Claim 2 wherein the

first and second contact pads each have a width that is about 3000 nm greater than a width of at least one of the first and second interconnects.

6. The thin film resistor as recited in Claim 2 wherein the first and second interconnects comprise aluminum.

7. The thin film resistor as recited in Claim 6 wherein the first and second interconnects comprise a titanium/titanium nitride/aluminum/titanium nitride stack.

8. The thin film resistor as recited in Claim 1 wherein the resistive layer includes tantalum nitride.

9. The thin film resistor as recited in Claim 8 wherein the resistive layer further includes tantalum pentoxide.

10. The thin film resistor as recited in Claim 1 wherein the first and second contact pads comprise a titanium/platinum stack.

11. The thin film resistor as recited in Claim 7 wherein the titanium/platinum stack includes titanium nitride located there between.

12. The thin film resistor as recited in Claim 1 wherein the resistive layer has a thickness ranging from about 20 nm to about 80 nm.

13. A method of fabricating a thin film resistor device, comprising:

forming a resistive layer on a first dielectric layer;

forming first and second contact pads on the resistive layer; and

forming a second dielectric layer over the resistive layer and the first and second contact pads.

14. The method as recited in Claim 13 further including forming a first interconnect that contacts the first contact pad and forming a second interconnect that contacts the second contact pad.

15. The method as recited in Claim 14 further including forming interconnect metallization structures wherein the first dielectric layer is formed between the interconnect metallization structure and the resistive layer.

16. The method as recited in Claim 15 wherein forming the first and second interconnects includes forming the first and second interconnects contacting the interconnect metallization structure.

17. The method as recited in Claim 14 wherein forming first and second contact pads includes forming first and second contact pads each have a width that is about 3000 nm greater than a width of at least one of the first and second interconnects.

18. The method as recited in Claim 14 wherein forming the first and second interconnects includes forming first and second aluminum interconnects.

19. The method as recited in Claim 18 wherein forming first and second aluminum interconnects includes forming first and second aluminum interconnects comprising a titanium/titanium nitride/ aluminum/titanium nitride stack.

20. The method as recited in Claim 13 wherein forming a resistive layer includes forming a tantalum nitride resistive layer.

21. The method as recited in Claim 20 wherein forming a resistive layer further includes forming a tantalum pentoxide layer.

22. The method as recited in Claim 13 wherein forming first

and second contact pads includes forming first and second contact pads comprising a titanium/platinum stack.

23. The method as recited in Claim 22 wherein forming first and second contact pads comprising a titanium/platinum stack includes forming first and second contact pads comprising a titanium/titanium nitride/platinum stack.

24. The method as recited in Claim 13 wherein forming a resistive layer includes forming a resistive layer having a thickness ranging from about 20 nm to about 80 nm.

25. An integrated circuit, comprising:

transistors;

interconnects formed in dielectric layers located over the transistors that interconnect the transistors to form an operative integrated circuit; and

a thin film resistor device interconnected to the transistors, including:

a resistive layer located on a first dielectric layer;

first and second contact pads located on the resistive layer; and

a second dielectric layer located over the resistive layer and the first and second contact pads.

26. The integrated circuit as recited in Claim 25 further including a first interconnect that contacts the first contact pad and a second interconnect that contacts the second contact pad.

27. The integrated circuit as recited in Claim 26 further including interconnect metallization structures wherein the first dielectric layer is located between the interconnect metallization structure and the resistive layer.

28. The integrated circuit as recited in Claim 27 wherein

each of the first and second interconnects contact an interconnect metallization structure.

29. The integrated circuit as recited in Claim 26 wherein the first and second contact pads each have a width that is about 3000 nm greater than a width of at least one of the first and second interconnects.

30. The integrated circuit as recited in Claim 26 wherein the first and second interconnects comprise aluminum.

31. The integrated circuit as recited in Claim 30 wherein the first and second interconnects comprise a titanium/titanium nitride/aluminum/titanium nitride stack.

32. The integrated circuit as recited in Claim 25 wherein the resistive layer includes tantalum nitride.

33. The integrated circuit as recited in Claim 32 wherein the resistive layer further includes tantalum pentoxide.

34. The integrated circuit as recited in Claim 25 wherein the first and second contact pads comprise a titanium/platinum stack.

35. The integrated circuit as recited in Claim 34 wherein the titanium/platinum stack includes titanium nitride located there between.

36. The integrated circuit as recited in Claim 25 wherein the resistive layer has a thickness ranging from about 20 nm to about 80 nm.

37. The integrated circuit as recited in Claim 25 wherein the transistors form part of a complementary metal oxide semiconductor (CMOS) device, bipolar device or BiCMOS device.